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EXAMINER
MALKOWSKI, KENNETH J

ART UNIT	PAPER NUMBER
2613	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/638,983	LEE ET AL.
	Examiner	Art Unit	
	Kenneth J. Malkowski	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2002*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,13,14 and 16-18* is/are rejected.

7)☒ Claim(s) *1,12 and 15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All   b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
   Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
   Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1.   Claim 1 is objected to because of the following informalities: The "drop interface"

referenced in claim 1, page 20 line 20 of applicants specification is claimed to be "arranged to

process the optical frames output from the wavelength division multiplexer to the IP router,"

however, it is clear from Figure 2 that the drop interface depicted in section 50 does not receive

any signals output from any WDM multiplexer. Appropriate correction is required.

Claim Rejections - 35 USC § 103

2.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

3.   Claim 1-4, 7, 9, 13-14 and 16-18 are rejected under 35 U.S.C. 103(a) as being

unpatentable over U.S. Patent No. 6,701,088 to Watanabe et al. in view of U.S. Patent

Application Publication No. 2002/0118241 to Xiong et al.

With respect to claim 1, Watanabe discloses an optical router (Figure 4) comprising: a

plurality of input ports (11-1, 11-2, Fig 4)(column 4 lines 10-14); a plurality of output ports (12-

1, 12-2, Fig 4); an add port (17-1,2,3 Fig 4) for inputting data received from a lower Internet

protocol (IP) router (16, Figure 4 (IP packet routing part)); a drop port (18-1,2,3 Fig 4) for

outputting data to the IP router (16, Figure 4 (IP packet routing part)); a wavelength division

demultiplexer arranged to wavelength-division-demultiplex wavelength signals input through the

input ports (11B, Fig 7 (wavelength demultiplexing circuit, located at each input shown in figure

4) and the add port [the add port shown in Figure 4 is functionally equivalent to an add port

including a wavelength-division-demultiplex circuit in that each signal entering (17-1, 17-2, 17-

3, Fig 4 (shown adding signals from IP packet router 16)) each add port is already split into

individual optical signals, thereby making the demultiplexer inconsequential to the functioning

of the optical router]; an input interface arranged to convert optical frames input from the

wavelength division demultiplexing section into electrical signals and also converting the

electrical signals to optical frames (13-1-13-6, Fig 4)(column 4 lines 16-23 (converts optical

paths to electrical signals and then restores the optical signal)); an optical switch for performing

a high-speed switching of the optical frames output from the input interface (14, Figure 4 (optical

path switch))(column 4 lines 36-39 (optical path switch)); an output interface arranged to process

the optical frames switched by and output from the optical switch (12-1, 12-2, Fig 4)(Figure 7A);

a wavelength division multiplexer arranged to wavelength-division-multiplex outputs of the

output interface section and transmit the multiplexed outputs to another optical router (12A, Fig

7A (optical path signal multiplexing circuit)); a drop interface arranged to process the optical

frames output from the optical switch to the IP router (18-1, 18-2, 18-3 Fig 4 (shown inputting

the dropped signals to the IP packet router 16)); a header processor arranged to recognize header

information and to control the optical router (column 5 lines 54-61 (overhead information

provides processing information such as connection control, administrative information, BER

monitoring, etc. and is stored in predetermined overhead areas OPS1-OPS3)); a header re-

inserter arranged to reinsert headers into outputs of the optical router (17B, Figure 5A (optical

path signal overhead insertion circuit)); and an edge traffic aggregator including of an ingress

part for converting IP packets input from the IP router (physical layer/IP conversion part 15,

Figure 4) into optical frames (column 3 lines 9-11 converting IP packets into optical path

signals)) and an egress part for converting the optical frames into IP packets (converting a

transmission signal input into IP packets and outputting the IP packets to routes corresponding to

their destinations)) and transmitting the converted packets to the lower IP router (IP/physical

layer conversion part 19, Fig 4). However, Watanabe fails to disclose an optical switch controller

arranged to control a connection state of the optical switch for switching the optical frames.

Xiong, from the same field of endeavor discloses a channel scheduling optical router (title)

which uses a non-blocking optical switch (24, Fig 1b), the same type of switch used in the

optical router as taught by Watanabe. Xiong further discloses using a switch controller (30, Fig

1b) for controlling said optical switch. Therefore, it would have been obvious to one of ordinary

skill in the art to implement the optical switch control as discloses by Xiong. The motivation for

doing so would have been to realize the obvious advantage of increased switching control for

purposes such as header switching. Xiong discloses using the switch controller (30, Fig 1b) in

the context of implementing configuration information extracted form packet headers (page 3

paragraph 54).

With respect to claim 2, Watanabe in view of Xiong disclose the optical router as claimed

in claim 1, wherein the wavelength division demultiplexer includes a plurality of wavelength

division de-multiplexers (Watanabe: WDM demultiplexer, 11B shown in Figure 7B is placed in

the plurality of units labeled 12-1 and 12-2 in Figure 4).

With respect to claims 3 and 17-18, Watanabe in view of Xiong disclose the optical

router as claimed in claim 1, wherein the input interface comprises: an optical receiver arranged

to convert an optical frame input from the wavelength division demultiplexer into an electrical

signal (Watanabe: 13-1-13-6, Fig 4)(Watanabe: column 4 lines 16-23 (converts optical paths to

electrical signals and then restores the optical signal)); a buffer coupled to the optical receiver

arranged to store the electrical signal for synchronization (Xiong: page 4 paragraph 69

(synchronization between headers and their associated data bursts))(Xiong: Figures 12, 13

(recirculation buffer 142, 144, 26)) (Xiong: page 2 paragraphs 28-29)(Xiong: page 3 paragraph

54 (scheduler (wherein the scheduler contains buffers as shown in Fig 12) tries to resynchronize

the header to its associated data burst)); a header length detector coupled to the optical receiver

and the buffer arranged to extract a header length in order to separate a header from the electrical

signal (Xiong: page 6 paragraph 91 (module contains frame counters and records the elapsed

frames since receiving the last header packet (hereinafter BHP). Upon receiving a BHP with an

arrival time, the frame is time-stamped and in the meantime a counter is reset to zero))(Xiong:

page 3 paragraph 53 (time stamp is the sum of the BHP arrival time)(Xiong: page 7 paragraph

101 (each BHP should contain a length field indicating the packet length from the first byte to

the last byte of the BHP in order to distinguish BHP's))(Xiong: page 4 paragraph 66 (based on

actual data burst departure time, reported, the BHP processor will pick the right time to send out

the BHP)); a switch coupled to the buffer arranged to separate the header and data from the

electrical signal (Watanabe: 18A, Fig 5B (optical path signal overhead separation

circuit))[although the header separated from data in Figure 5B occurs in the optical domain,

these two techniques are functionally equivalent in that the action of separating a header from

data is performed. Whether the signal is optical or electrical does not change the this equivalent

function]; a queue coupled to the switch arranged to store data separated by the switch (Xiong:

80, Figure 3 (Queue is shown receiving an input "from switch" and sending header information

to header processor 82))(page 4 paragraph 64 (BHP's arriving from the electronic switch are first

stored in scheduling queue 80)); an optical transmitter coupled to the queue arranged to restore

the electrical signal an optical frame in order to transmit the data to the optical switch (Xiong:

46, Figure 3 (BHP transmitter module, which is coupled to an electro-optic converter 48 to

restore the electrical signal into an optical as shown in Figure 1b)); a header processor (Xiong:

82, Figure 3 (BHP processor)) arranged to read an address with reference to the header of the

electrical signal and determine a header output time (Xiong: page 4 paragraph 64 (BHP

processor coordinates the data and control channel scheduling process and sends the

configuration to the path and channel scheduling selector)); and a header reinserting section

arranged to insert a new header output from the header processor (Xiong: page 3 paragraph 54

(scheduler schedules the transmission of the headers so that they are resynchronized with their

associated data bursts))(Watanabe: 17B, Figure 5A (overhead insertion circuit)).

With respect to claim 4, Watanabe in view of Xiong disclose the optical router as claimed

in claim 3, wherein a predetermined guard time is provided between the header separated from

the switch and the data frame in order to prevent data loss when the header and the data frame

are separated (Xiong: page 1 paragraph 20)(Xiong: Figures 4A, 4B which show the offset time

between the header and the data)(Xiong: page 2 paragraph 46 (the BHP is set ahead of its

associated data burst with an offset time)).

With respect to claim 7, Watanabe in view of Xiong disclose the optical router as claimed

in claim 1, wherein the input interface comprises: an optical receiver arranged to convert optical

frames input from the wavelength division demultiplexer into electrical signals (13-1-13-6, Fig

4)(column 4 lines 16-23 (converts optical paths to electrical signals and then restores the optical

signal)); a buffer coupled to the optical receiver and arranged to store the electrical signals

(Xiong: Figures 12, 13 (recirculation buffer 142, 144, 26)) (Xiong: page 2 paragraphs 28-

29)(Xiong: page 3 paragraph 54 (scheduler (wherein the scheduler contains buffers as shown in

Fig 12) tries to resynchronize the header to its associated data burst)); a header length detector

coupled to the optical receiver and arranged to extract a header length in order to separate

headers from the electrical signal Xiong: page 7 paragraph 101 (each BHP should contain a

length field indicating the packet length from the first byte to the last byte of the BHP in order to

distinguish BHP's))(Xiong: page 4 paragraph 66 (based on actual data burst departure time,

reported, the BHP processor will pick the right time to send out the BHP)); a switch coupled to

the buffer and arranged to separate the headers and data from the electrical signals (Watanabe:

18A, Fig 5B (optical path signal overhead separation circuit))[although the header separated

from data in Figure 5B occurs in the optical domain, these two techniques are functionally

equivalent in that the action of separating a header from data is performed. Whether the signal is

optical or electrical does not change the this equivalent function]; a queue coupled to the switch

and arranged to store data separated by the switch (Xiong: 80, Figure 3 (Queue is shown

receiving an input "from switch" and sending header information to header processor 82))(page

4 paragraph 64 (BHP's arriving from the electronic switch are first stored in scheduling queue

80)); a plurality of optical transmitters arranged to input data from the queue and to restore the

electrical signals to optical frames in order to transmit the data to the optical switch (Xiong: 46,

Figure 3 (BHP transmitter modules, which are coupled to electro-optic converters 48 to restore

the electrical signal into an optical as shown in Figure 1b)); a header processor (Xiong: 82,

Figure 3 (BHP processor)) arranged to read addresses with reference to the headers of the

electrical signals and deciding header output times (Xiong: page 4 paragraph 64 (BHP processor

coordinates the data and control channel scheduling process and sends the configuration to the

path and channel scheduling selector)); and a header reinserting section arranged to insert new

headers output from the header processor (Xiong: page 3 paragraph 54 (scheduler schedules the

transmission of the headers so that they are resynchronized with their associated data

bursts))(Watanabe: 17B, Figure 5A (overhead insertion circuit)).

With respect to claims 9, Watanabe in view of Xiong disclose the optical router as

claimed in claim 1, wherein the output interface comprises: an optical receiver arranged to

convert the optical data switched by the optical switch into an electric signal (Watanabe: 13-1-

13-6, Fig 4)(Watanabe: column 4 lines 16-23 (converts optical paths to electrical signals and

then restores the optical signal)); a buffer arranged to temporarily store the data for a header

reinsertion (Xiong: page 4 paragraph 69 (synchronization between headers and their associated

data bursts))(Xiong: Figures 12, 13 (recirculation buffer 142, 144, 26)) (Xiong: page 2

paragraphs 28-29)(Xiong: page 3 paragraph 54 (scheduler (wherein the scheduler contains

buffers as shown in Fig 12) tries to resynchronize the header to its associated data burst))

(Watanabe: column 5 lines 54-61 (overhead information provides processing information such as

connection control, administrative information, BER monitoring, etc. and is stored in

predetermined overhead areas OPS1-OPS3)); a header re-inserter arranged to reinsert the header

(Watanabe: 17B, Figure 5A (optical path signal overhead insertion circuit)); and an optical

transmitter arranged to transmit the optical data combined with the header to a next node ((12-1,

12-2, Fig 4)(Figure 7A).

With respect to claim 13, Watanabe in view of Xiong disclose the optical router as

claimed in claim 1, wherein the egress part of the edge traffic aggregator comprises: a

wavelength division demultiplexer arranged to wavelength-division-demultiplex the wavelength-

division-multiplexed optical signal dropped by the optical router (Watanabe: signals exiting

routing part 18 and are sent to IP/Physical layer conversion part 19 are the dropped optical

signals)[the drop port shown in Figure 4 is functionally equivalent to a drop port including a

wavelength-division-demultiplex circuit in that each signal entering (18-1, 18-2, 18-3, Fig 4

(shown dropping signals to IP packet router 16)) each drop port is already split into individual

optical signals, thereby making the demultiplexer inconsequential to the functioning of the

optical router]; a plurality of optical receivers arranged to convert the optical frame into the

electric signal (Watanabe: column 4 lines 48-52 (optical path signals are fed to optical path

signal/IP conversion parts to restore IP packets which are electrical signals)); a data frame

disassembler arranged to separate the frame in a unit of an IP packet and then separate the frame

by destinations (column 4 lines 52-58 (IP packet routing part distributes IP packets to routes

according to their destinations)); a scheduler arranged to control an output order of IP packets

separated by destinations (Wiong: 42, Figure 1b (scheduler)); a plurality of packet processor

arranged to process the IP packets through at least a forwarding process (Wiong: 36, Figure 1b

(packet processor)); an address table coupled to the plurality of packet processors; an electric

switch coupled to the plurality of packet processors (Xiong: pave 3 paragraph 53 (forwarder

mainly performs forwarding table lookup to decide which outgoing CCG to forward to the

BHP)); and a plurality of optical transmitters arranged to optically modulate the switched packets

(Xiong: 46, Fig 1b (transmit module, which is sent to optical signal converter 48)).

With respect to claim 14, Watanabe in view of Xiong disclose the optical router as claimed in claim 1, wherein the edge traffic aggregator converts the packets input from the IP router into the optical frames of a predetermined length according to addresses of destinations (Watanabe: 17-1,2,3 Figure 4 (labeled IP to optical signal converter)), the input interface processes the optical frames through an optical/electric/optical conversion (Xiong: units 34 and 48 perform said optical/electric/optical conversion in Figure 1b)), the optical switch performs a switching of the optical frames (Watanabe: 14, Figure 14)(Xiong: 24, Figure 1b), and the output interface processes the optical frames through the optical/electric/optical conversion (Xiong: units 34 and 48 perform said optical/electric/optical conversion in Figure 1b)) and then transmits the optical frames to a next optical router node (Watanabe: signals sent to ops signal/ otm converter 12-1,2 Figure 4) or the edge traffic aggregator (Watanabe: signals sent to optical signal / IP converter 18-1,2,3 Figure 4).

4.   Claims 5-6, 8, and 10-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,701,088 to Watanabe et al. in view of U.S. Patent Application Publication No. 2002/0118241 to Xiong et al. and further in view of U.S. Patent Application Publication No. 2002/0018468 to Nishihara et al.

With respect to claims 5-6, Watanabe in view of Xiong disclose the optical router as claimed in claim 3, wherein the queue (80, figure 3) of the input interface comprises buffers (84, 82 Figure 3)(142, 144 Figure 12) arranged to receive and store the data (page 6 paragraph 91). However, Watanabe in view of Xiong fail to disclose a plurality of buffers wherein the buffers include at least one buffer for each possible destination. Nishihara, from the same field of endeavor discloses a plurality of buffers (Figure 10 (buffer section))(Figure 7 (buffer for each

path)) arranged to receive and store the data by destinations (page 4 paragraph 62 (individual

buffers or memories are provided for respective paths))(page 5 paragraph 76 (frame length and

transfer are defined individually for each path corresponding to user traffic)), a combiner coupled

to the plurality of buffers (Figure 7, immediately after said plurality of buffers, signals are

combined), as well as an electrical switch for selecting channels for transmission to each

destination (page 2 paragraph 21). Therefore, it would have been obvious to one of ordinary skill

in the art to implement a plurality of buffers arranged to receive and store data by destinations as

taught by Nishihara into the buffering system as taught by Watanabe in view of Xiong. One

motivation for doing so is the suggestion made by the combination of Watanabe in view of

Xiong that the buffers could be arranged in parallel depending on desired implementation

(Xiong: page 4 paragraph 64 depending on desired implementation)). A further motivation

would have been that doing so increases flexibility for data transmission on each optical channel

in a WDM network (page 3 paragraph 17) and that quality of signal issues can be addressed on

an individual user basis, thereby providing a better quality of service for each customer (page 5

paragraph 76).

With respect to claims 8, Watanabe in view of Xiong disclose the optical router as

claimed in claim 7, however fail to specifically disclose the buffer includes a plurality of outputs.

Nishihara, from the same field of endeavor discloses a buffer section with a plurality of outputs

(11, Figure 2 (buffer section 11 has a plurality of outputs))(abstract (buffer section comprised of

plural buffers)). Therefore, it would have been obvious to one of ordinary skill in the art to

implement a plurality of buffers arranged to receive and store data by destinations as taught by

Nishihara into the buffering system as taught by Watanabe in view of Xiong. One motivation for

doing so is the suggestion made by the combination of Watanabe in view of Xiong that the

buffers could be arranged in parallel depending on desired implementation (Xiong: page 4

paragraph 64 depending on desired implementation)). A further motivation would have been that

doing so increases flexibility for data transmission on each optical channel in a WDM network

(page 3 paragraph 17) and that quality of signal issues can be addressed on an individual user

basis, thereby providing a better quality of service for each customer (page 5 paragraph 76).

With respect to claims 10, Watanabe in view of Xiong disclose the optical router as

claimed in claim 1, wherein the output interface comprises: a plurality of optical receivers

arranged to convert the optical data switched by the optical switch into electric signals

(Watanabe: 13-1-13-6, Fig 4)(Watanabe: column 4 lines 16-23 (converts optical paths to

electrical signals and then restores the optical signal)); a buffer to couple the plurality of optical

receivers, respectively, and arranged to temporarily store the data output from the plurality

optical receivers for a header reinsertion (Xiong: page 4 paragraph 69 (synchronization between

headers and their associated data bursts))(Xiong: Figures 12, 13 (recirculation buffer 142, 144,

26)) (Xiong: page 2 paragraphs 28-29)(Xiong: page 3 paragraph 54 (scheduler (wherein the

scheduler contains buffers as shown in Fig 12) tries to resynchronize the header to its associated

data burst)); a header re-inserter arranged to reinsert the header (Watanabe: 17B, Figure 5A

(optical path signal overhead insertion circuit)); and an optical transmitter arranged to transmit

the optical data combined with the header to a next node (Watanabe: 12A, Fig 7A (optical path

signal multiplexing circuit)). However, Watanabe in view of Xiong fail to disclose a plurality of

buffers. . Nishihara, from the same field of endeavor discloses a plurality of buffers (Figure 10

(buffer section))(Figure 7 (buffer for each path)) arranged to receive and store the data by

destinations (page 4 paragraph 62 (individual buffers or memories are provided for respective

paths))(page 5 paragraph 76 (frame length and transfer are defined individually for each path

corresponding to user traffic)), a combiner coupled to the plurality of buffers (Figure 7,

immediately after said plurality of buffers, signals are combined), as well as an electrical switch

for selecting channels for transmission to each destination (page 2 paragraph 21). Therefore, it

would have been obvious to one of ordinary skill in the art to implement a plurality of buffers

arranged to receive and store data by destinations as taught by Nishihara into the buffering

system as taught by Watanabe in view of Xiong. One motivation for doing so is the suggestion

made by the combination of Watanabe in view of Xiong that the buffers could be arranged in

parallel depending on desired implementation (Xiong: page 4 paragraph 64 depending on desired

implementation)). A further motivation would have been that doing so increases flexibility for

data transmission on each optical channel in a WDM network (page 3 paragraph 17) and that

quality of signal issues can be addressed on an individual user basis, thereby providing a better

quality of service for each customer (page 5 paragraph 76).

With respect to claim 11, Watanabe in view of Xiong disclose the optical router as

claimed in claim 1 (Watanabe: Figure 4), wherein the ingress part of the edge traffic aggregator

comprises: a plurality of optical receivers arranged to receive packet data input from the lower IP

router (17-1,2,3 Figure 4 (shown connected to lower IP routing inputs L11-L13)); a plurality of

packet processors coupled to the plurality of optical receivers, respectively, and arranged to

perform at least a packet forwarding function (36, Figure 1b, (packet processors))(page 3

paragraph 53 (packet processor performs various functions including forwarding)); an address

table coupled to the plurality of packet processors (Xiong: pave 3 paragraph 53 (forwarder

mainly performs forwarding table lookup to decide which outgoing CCG to forward to the

BHP)); an electric switch coupled to the plurality of packet processors (Xiong: 40, Figure 1b); a

data frame assembler (page 2 paragraph 45 (burst assembly and disassembly functions)); a

controller and scheduler arranged to determine output orders (Xiong: page 3 paragraph 54

(scheduler (wherein the scheduler contains buffers as shown in Fig 12) tries to resynchronize the

header to its associated data burst)); an electric switch arranged to transmit the optical data of

which the output order and the wavelength are determined (Xiong, 40, Figure 1b); a

predetermined number of header inserting sections arranged to insert the header before an optical

modulation (Watanabe: 17B, Figure 5A (overhead insertion circuit located in each transmitter));

an optical transmitting section including n optical transmitters arranged to optically modulate the

optical frames combined with the headers (Watanabe: 17-1,2,3 Figure 4) (Watanabe: 17, Figure

5A (laser light source is located after the header is inserted into the data packet)) and a

wavelength division multiplexer arranged to wavelength-division-multiplexing the optically

modulated signals (Watanabe: 12A, Figure 7A (multiplexing circuit))((Watanabe: 54-1,2,3,4

Figure 2)). However, Watanabe in view of Xiong fail to disclose a predetermined number of

buffers arranged to convert switched packets into the optical frames. Nishihira, from the same

field of endeavor discloses a predetermined number of buffers (Figure 7 (buffer for each path)

arranged to convert switched packets into the optical frames (Figure 7 (frame switching

section)). Therefore, it would have been obvious to one of ordinary skill in the art to implement a

predetermined plurality of buffers arranged to convert switched packets into optical frames as

taught by Watanabe in view of Xiong. One motivation for doing so is the suggestion made by the

combination of Watanabe in view of Xiong that the buffers could be arranged in parallel

depending on desired implementation (Xiong: page 4 paragraph 64 depending on desired implementation)). A further motivation would have been that doing so increases flexibility for data transmission on each optical channel in a WDM network (page 3 paragraph 17) and that quality of signal issues can be addressed on an individual user basis, thereby providing a better quality of service for each customer (page 5 paragraph 76).

Allowable Subject Matter

5.   Claims 12 and 15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6.   The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following references are cited to show the state of the art with respect to optical signal and IP routing in general:

U.S. Patent 6,786,827 is cited to show an integrated optical router with O/E/O conversion at each input and output

U.S. Patent Application Publication No. 2004/0105675 is cited to show header/ frame detection in an optical packet router

U.S. Patent Application Publication No. 2002/0109878 is cited to show a labeled optical burst switching for IP-over-WDM integration

U.S. Patent Application Publication No. 2002/0145786 is cited to show an optical layer multicast switch with label switching, add/drop function

7.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kenneth J. Malkowski whose telephone number is (571) 272-5505. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KJM 8/17/06

KENNETH VANDERPUYE
SUPERVISORY PATENT EXAMINER